REMARKS

Claims 1, 3-9, 11 and 12 are pending in the present application, were examined, and stand rejected. In response, Claims 1, 3 and 9 are amended, Claims 5-8 are cancelled and Claims 16-25 are added.. Applicant respectfully requests reconsideration of pending Claims 1, 3-4, 9, 11, 12 and 16-25 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Objection to the Specification

The Examiner has objected to page 5, lines 3-4 (paragraph [0017]) of the disclosure for an informality. Applicant has amended the paragraph [0017] to overcome the objection

II. Claims Rejected Under 35 U.S.C. §112

The Examiner has rejected Claims 1, 3-9 and 11-12 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Regarding Claims 1 and 9, Claims 1 and 9 have been amended to replace the phrase "an off-chip memory module" with an off-chip system memory. The off-chip system memory is illustrated with reference to Figs. 1 and 2 of Applicant's specification. Applicant respectfully submits that the term "off-chip" generally refers to components that are not integrated onto the motherboard of a computer system. Accordingly, Applicant respectfully submits that the recited feature of Claims 1 and 9 to an off-chip system memory are described by the Applicant's specification at the time of filing.

Regarding Claim 9, Claim 9 recites "a data cache including an eviction buffer". Applicant amends claims to replace the recited feature as follows: a data cache coupled to an eviction buffer. The data cache coupled to the eviction buffer is illustrated with reference to Fig. 5 of Applicant's specification wherein data cache 530 is coupled to eviction buffer 540. Accordingly, Applicant respectfully submits that Applicant's specification, at the time of filing, clearly disclosed the recited feature of a data cache coupled to an eviction buffer.

Accordingly, Applicant respectfully submits that in view of Applicant's amendments, Claims 1, 3-4, 9 and 11-12 comply with the written description requirement under 35 U.S.C. §112, first paragraph. Accordingly, Applicant respectfully requests the Examiner reconsider and withdraw the 35 U.S.C. §112, first paragraph rejection of Claims 1, 3-4, 9 and 11-12.

The Examiner has rejected Claim 3 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In response, Applicant has amended Claim 3 to recite "memory device of the memory module." Accordingly, Applicant respectfully submits that Claim 3 is amended particularly points out and distinctly claims the subject matter which Applicant regards as the

invention. Consequently, Applicant respectfully requests the Examiner reconsider and withdraw the 35 U.S.C. §112, second paragraph rejection of Claim 3.

III. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 1, 3-9 and 11-12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,216,178 issued to Stracovsky et al. ("Stracovsky") in view of U.S. Patent No. 6,128,702 issued to Saulsbury et al. ("Saulsbury"). Applicant respectfully traverses this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Claim 1 is amended to recite the following claim feature, which is neither taught nor suggested by either Stracovsky or Saulsbury, whether reviewed alone or in combination:

> a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory module of an off-chip system memory, the memory controller coupled to the memory module via a memory bus, the command sequencer and serializer unit to cause a current line of data to be written from the command sequencer and serializer unit to the data cache, the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to the eviction buffer located on the memory module. (emphasis added.)

As correctly pointed-out by the Examiner, Stracovsky differs from the claimed invention and not specifically [sic] teaches a data cache located on the memory module and the command sequencer and serial unit to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module. (*See*, paper no. 3 of Office Action mailed March 24, 2004.) Accordingly, the Examiner cites Saulsbury, which according to the Examiner, teaches the above-described features of Claim 1 prior to amendment.

Contrary to Applicant's invention, as well as Stracovsky, Saulsbury is directed:

> An integrated P/M device 100 in accordance with the present invention. The integrated components of the P/M device include a CPU 102, an on-chip memory system 103, a 64-bit data bus 108, a 25-bit data address bus 110, a 32-bit instruction bus 112, a 25-bit instruction address bus 114 and a control bus 116. The memory system includes 16 memory blocks 104 and a victim cache 106. (col. 3, lines 46-53.) (emphasis added.)

Conversely, Claim 1, as amended, recites an off-chip (non-integrated) system memory including at least one memory module. Furthermore, as indicated by the cited passage of Saulsbury, Saulsbury teaches that the integrated memory system includes 16 memory blocks and a single victim cache 106. Conversely, Claim 1, as amended, recites a data and eviction buffer per memory module of an off-chip system memory. Accordingly, Applicant respectfully submits that the Examiner fails to establish a *prima facie* case of obviousness of Claim 1, as amended, since the combination of Stracovsky in view of Saulsbury fails to teach or suggest each of the features of Claim 1, as amended.

Furthermore, Applicant respectfully submits that the Examiner fails to illustrate a suggestion or motivation to modify the teachings of Stracovsky in view the teachings of Saulsbury. Applicant respectfully submits that the lack of such a suggestion or motivation is based on the fact that Stracovsky deals with problems faced by:

> Systems in which many components (processors, hard drive, etc.) must share a common bus in order to access memory presence [sic] there is a high probability of memory access conflicts. (col. 1, lines 37-40.) (emphasis added.)

Applicant respectfully submits that the teachings of Stracovsky refer to off-chip memory systems, which are generally coupled to a processor and corresponding chipset via a memory bus. Conversely, as indicated above, Saulsbury is directed to an integrated processor/memory device comprising a main memory, a CPU, a victim cache and a primary cache (*See*, Abstract). Applicant respectfully submits that one skilled in the art would not look to a reference such as Saulsbury, which teaches an integrated processor memory device to solve problems associated with off-chip system memory, as described in the Background of Stracovsky.

Applicant respectfully submits that the Examiner has engaged in an improper hindsight based analysis to combine the teachings of Stracovsky in view Saulsbury. Consequently, Applicant respectfully submits that the Examiner fails to establish that it would be obvious to combine the missing elements provided by Saulsbury with the teachings of Stracovsky.

Therefore, Applicant respectfully submits that the Examiner fails to establish a *prima facie* case of obviousness of Claim 1, as amended, since the Examiner fails to illustrate a teaching or suggestion to modify or combine the reference teachings of Stracovsky in view of Saulsbury and also fails to illustrate a teaching or suggestion of each of the above-recited features of amended Claim 1, based on the combination of Stracovsky in view of Saulsbury.

Applicant respectfully submits that Claim 1, as amended, is patentable over Stracovsky, Saulsbury and the references of record, whether viewed alone or in combination. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 1.

Regarding Claims 3 and 4, Claims 3 and 4 depend from Claim 1 and therefore include the patentable claim features of Claim 1, as described above. Accordingly, Claims 3 and 4, based on their dependency from Claim 1, are also patentable over the combination of Stracovsky in view of Saulsbury, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 3 and 4.

Regarding Claim 9, Claim 9 is amended to recite the following claim feature which neither taught or suggested by the combination of Stracovsky in view of Saulsbury:

> an off-chip system memory coupled to the memory controller, the off-chip system memory including at least two memory modules, each memory module including
> at least one memory device, and
> a data cache coupled to an eviction buffer, each coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from a data cache into the eviction buffer.

Applicant respectfully submits that Claim 9 is amended to illustrate a system memory that includes at least two memory modules with each memory module including its own data cache and eviction buffer. Conversely, as described above with reference to Claim 1, the combined teachings of Stracovsky in view of Saulsbury teach an integrated system which includes 16 memory banks 104 and single victim data cache 106. Accordingly, Applicant respectfully submits that Applicant's amendment to Claim 9 prohibits the Examiner from establishing a *prima facie* case of obviousness to Claim 9 over Stracovsky in view of Saulsbury, since the combination fails to teach or suggest each of the recited features of amended Claim 9.

Furthermore, as indicated above, the Examiner fail to show suggestion or a motivation to combine the reference teachings of Stracovsky, which is directed to problems associated with off-chip system memory, with Saulsbury which teaches an integrated processor and memory device (*See* Saulsbury, lines 46-53); and hence, is not directed to problems associated with off-chip system memory. Therefore, Applicant respectfully submits that the Examiner has engaged in an improper hindsight based analysis to render the recited features of Claim 9 obvious.

Consequently, Applicant respectfully submits that amended Claim 9 is patentable over the combination of Stracovsky in view of Saulsbury as well as the references of record. Applicant respectfully requests the Examiner reconsider and withdraw the §103(a) rejection of Claim 9.

Regarding Claims 11 and 12, Claims 11 and 12, based on their dependency from Claim 9, are also patentable over the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 11 and 12.

Regarding new Claims 16 and 20, new Claims 16 and 20 recite:

> a writeback command, the writeback command to cause the previous line of data to be written out of the eviction buffer to the memory device. (emphasis added.)

Applicant respectfully submits that Saulsbury specifically teaches away from the above recited feature. As indicated by Saulsbury:

> The victim data cache is used to store victim data cache sub-line (or sub-locks) of primary data cache lines that were recently replaced (i.e., or replacement victims) with new primary data cache lines in the primary data cache banks 122 (Column 8, lines 5 to 9),

However, when a read operation is detected, data is not written from the victim data cache 106 to main memory banks 118. As indicated by Saulsbury:

> When the W/R signal received from the ÇPU 102 indicates that a write is occurring ... the data word that is written or read at the memory location specified by the issue data address must be written to or read from the primary data cache bank 122 in the main memory block 104 with the corresponding main memory bank 118 that has the memory location specified by the issue data address (Column 9, lines 29 - 39),

As further described within Saulsbury, the writing of data to main memory banks 118 is performed from the primary cache banks 122 and not from the victim data cache 106. As described within Saulsbury:

> Prior to replacing the victim data cache line with a new data cache line, the primary data cache bank control state machine 152 writes back to the corresponding main memory bank 118 the victim primary data cache line if it is dirty (state 163 of Fig. 6), ,,, If it is dirty, then the primary data cache bank control state machine issues on the control bus a dirty cache line read signal indicating that it needs to write back a dirty victim primary cache line (Column 12, line 48 - 60).

Accordingly, Applicant respectfully submits that the victim data cache 106, based on the cited passages above, is not used to write data to a memory device in response to a writeback command as recited by new Claims 16 and 19.

Hence, Applicant respectfully submits that the combination of Stracovsky in view of Saulsbury would fail to teach the above recited features of Claims 16 and 19 as well as dependent Claims 17-19 and 21-22.

Regarding new Claim 23, new Claim 23 describes a system memory wherein the system memory includes at least two memory modules with each memory module including a data cache and an eviction cache. For at least the reasons described with reference to Claims 1 and 9, the combination of Stracovsky in view of Saulsbury would fail to teach such features of Claim 22 and dependent Claims 24-25. Accordingly, Applicant respectfully requests that the Examiner allow new Claims 16 - 25.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1, 3-4, 9, 11 12 and 16-25, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: December 29 2004

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Linda Black 12/29/2004
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